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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/450,802	11/29/1999	JAY SETHURAM	STRAT-P013	8198

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EXAMINER	
DUONG, DUC T	
ART UNIT	**PAPER NUMBER**
2663	8

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/450,802	SETHURAM, JAY	
	Examiner	Art Unit	
	Duc T. Duong	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 14-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Inventorship

1. In view of the papers filed June 7, 2000, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by adding the addition of Richard Weber and Chandra Joshi as inventors.

The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of the file jacket and PTO PALM data to reflect the inventorship as corrected.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6, 7, 9-11, and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa (U.S. Patent 5,748018).

Regarding to claim 1, Ishikawa discloses a source synchronous clocking system (Fig. 3A), comprising a source clock domain in a first layer 100 (Fig. 3A), comprising a register 101 having a first input D for receiving a data signal (Fig. 2A col. 4 lines 2-3), a second input CK for receiving a clock signal (Fig. 2A col. 4 lines 3-5), and an output Q

(Fig. 2 A col. 4 lines 5-8); and a buffer 103 having an input CLK for receiving the clock signal and an output 105 (Fig. 2A col. 4 lines 10-14), said buffer generating a delay that is substantially equivalent to a delay through said register (col. 4 lines 29-33); and a destination clock domain in a second layer 200 (Fig. 3A), comprising a register 201 having a first input D and a second input CK, the first input of said register of said destination clock domain being coupled to the output of said register in the source clock domain (Fig. 3A col. 4 lines 47-49).

Regarding to claim 2, Ishikawa discloses the source clock domain 100 comprises a first transmit clock 104 domain in the first layer for transmitting the data and clock signals (Fig. 3A col. 4 lines 3-5) to the said destination clock domain 200 that comprises a transmit clock 203 domain in the second layer (Fig. 3A col. 4 lines 45-47), said first layer comprising a link layer, said second layer comprising a PHY layer (Noted the implementation of link layer and physical layer is inherent in the interconnection between the various components of the integrated circuit shown in Fig. 3A).

Regarding to claim 3, Ishikawa discloses the source clock domain 100 comprises a first receive domain (the inputs D and CK form the first receive domain) said the first layer for transmitting data and clock signals (Fig. 3A col. 4 lines 1-5) to said destination clock 200 that comprises a receive clock domain (the inputs D and CK form the second receive domain) in said second layer (Fig. 3A col. 4 lines 41-47), said first layer including a PHY layer, said second layer including a link layer.

Regarding to claim 4, Ishikawa discloses a delay circuit (implicitly shown), coupled between said source clock domain and said destination clock domain, for introducing additional delay to the clock signal (Fig. 2A col. 4 lines 10-14).

Regarding to claim 6, Ishikawa discloses a serial termination circuit (Fig. 4A; one of terminating resistor 322 and 326 form a serial termination circuit) for absorbing a reflection generated by the data signal (col. 7 lines 10-16).

Regarding to claim 7, Ishikawa discloses a parallel termination circuit (Fig. 4A; both terminating resistor 322 and 326 form a parallel termination circuit) for absorbing a reflection generated by the data signal (col. 7 lines 10-16).

Regarding to claim 9, Ishikawa discloses a method for operating a source synchronous clocking system between a first layer and a second layer from a source clock (Fig. 3A), comprising receiving an input clock signal CK in a first clock domain in a first layer 100 (Fig. 2A col. 4 lines 3-5); receiving an input data signal D in the first clock domain in the first layer (Fig. 2A col. 4 lines 2-3); sourcing the input clock signal and the input data signal from a source clock CLK (col. 4 lines 3-5), the source clock triggering the input clock signal and the input data signal (Fig. 2B col. 4 lines 14-28); and generating an output clock signal 105 and an output data signal 106 in the second clock domain in the second layer 200 (Fig. 3A col. 4 lines 41-47), the output clock signal and the output data signal being synchronized to each other (Fig. 3b col. 4 lines 55-65).

Regarding to claims 10 and 11, Ishikawa discloses the first layer comprises a link layer and the second layer comprises a PHY layer (Noted the implementation of link layer and physical layer is inherent in the interconnection between the various

components of the integrated circuit shown in Fig. 3A), the input clock and data signal being transferred from the link layer to the PHY layer or from PHY layer to link layer (Fig. 3A col. 4 lines 47-50).

Regarding to claim 14, Ishikawa discloses a method for sourcing a clock input and a data input synchronously between a link layer and a PHY layer (Fig. 3A; Noted the implementation of link layer and physical layer is inherent in the interconnection between the various components of the integrated circuit shown in Fig. 3A), the link layer including a transmit clock domain 105 and a receive clock domain (the inputs D and CK of 100 form the first receive domain), the PHY layer including a transmit clock domain 203 and a receive clock domain (the inputs D and CK of 200 form the second receive domain), comprising the steps of receiving the clock input CK (Fig. 2A col. 4 lines 3-5); receiving the data input D (Fig. 2A col. 4 lines 2-3); transmitting the clock input to a latching device for triggering the data input (Fig. 3B col. 4 lines 55-62); sending the clock input through a buffer (Fig. 3A col. 4 lines 5-8), the buffer having a delay which is equal to the delay through the latching device (col. 4 lines 10-14); and generating an output data from the latching device that synchronizes with an output clock from the buffer (Fig. 3B col. 4 lines 55-65).

Regarding to claim 15, Ishikawa discloses the transmitting step comprises transmitting the clock input from a link layer to a PHY layer (Fig. 3A col. 4 lines 10-14).

Regarding to claim 16, Ishikawa discloses the transmitting step comprises transmitting the clock input from a PHY layer to a link layer (Fig. 3A col.4 lines 41-47).

Regarding to claim 17, Ishikawa discloses the step of merging the clock signal 105 at the PHY layer to a clock input 204 at the PHY layer (Fig. 3A col. 4 lines 41-47).

Regarding to claim 18, Ishikawa discloses the step (Fig. 4A; one of terminating resistor 322 and 326 form a serial termination circuit) for absorbing a reflection generated from the data input by serial termination circuit (col. 7 lines 10-16).

Regarding to claim 19, Ishikawa discloses the step (Fig. 4A; both terminating resistor 322 and 326 form a parallel termination circuit) for absorbing a reflection generated from the data input by parallel termination circuit (col. 7 lines 10-16).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 8, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa in view of Nichols et al (U.S. Patent 6,356,557 B1).

Regarding to claims 5, 8, and 20, Ishikawa disclose all the limitation with respect to claim 1, except for a second buffer having an input coupled to the output of said delay circuit and an output coupled to said register in said destination clock domain (claim 5); the clock signal generated from the output of the second buffer being connected to a clock input of in said destination clock domain (claim 8); and generating control signals of a the data input, the control signals being multiplexed with the data input (claim 20).

However, Nichols discloses a UTOPIA interface comprises a second buffer 79 having an input coupled to the output of said delay circuit 74 and an output coupled to said register 88 in said destination clock domain (Fig. 3A col. 3 lines 11-18); the clock signal generated from the output of the second buffer 79 being connected to a clock input of in said destination clock domain 88 (Fig. 3A col. 3 lines 16-21); and generating control signals of a the data input, the control signals being multiplexed with the data input (Fig. 3A col. 3 lines 46-55).

Thus, it would have been obvious to one of ordinary skilled in the art, at the time of the invention, to include the UTOPIA interface as taught by Nichols in Ishikawa's system to permits transmission of data at a high clock rate.

Response to Arguments

6. Applicant's arguments filed November 29,1999 have been fully considered but they are not persuasive. Regarding to Applicant's argument on pages 10-11 that Ishikawa does not teach for the buffer generating a delay that is **substantially** equivalent to a delay though said register is direct to previously cited portion again. Since Ishikawa already discloses the buffer generating a delay coincide with the flip flop, the term **substantially** equivalent has been given the broadest interpretation in considering the buffer delay **close** equivalent to the flip flop delay for any values. Thus, based on the reason set forth in the above, the rejection remains held.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Duong whose telephone number is 703-605-5146. The examiner can normally be reached on M-Th (8:30 AM-5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 703-308-5340. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DD
September 23, 2003

STEVEN H.D NGUYEN
PRIMARY EXAMINER